Horns set to lock?

US government set to clash with technology community? **Paul Dempsey** reports.

Intel's plan for its first Chinese fab may be a forerunner of conflict between the US government and the semiconductor industry.

Fab 68, set to open in 2010, will be a 300mm wafer plant 'initially' producing chipsets, but not microprocessors. Intel has confirmed with Washington that this project does not breach US technology transfer restrictions.

However, politicians want to know Intel's longer term plans for the $2.5billion site. China is silicon's fastest growing market and it would make economic sense for Intel and others to have cutting edge production capacity in the region. The backdrop to their concern also takes its cue from the broader trend towards globalisation in semiconductor research.

"We not only have Intel, but also TI and the ex Motorola guys [Freescale] moving more manufacturing and R&D to Asia," said a senior Capitol Hill aide, referring to recent decisions by several chip manufacturers to outsource process development to foundries such as TSMC.

The aide said the trend raised two issues. "Companies tell us they will stick to the rules, but it is difficult to manage traffic in that kind of information. Sometimes, people have to instantly decide whether they can share something or not with millions of dollars at stake," he said.

"And there are security issues. During the Cold War, the country saw technological primacy as a priority. Now, we are at war again. The more of this research that is shared, the less there will be that we hold closely. For semiconductors, sensitive technology may not immediately appear to have a direct military or security connection."

Washington's sensitivities were highlighted publicly last month when military contractor ITT was hit with the largest ever technology transfer fine – $100million – after details of night vision equipment were disclosed to low cost suppliers in China and other countries.

Following the ITT judgement, a major review of US technology transfer regulations and their enforcement looks likely.

Asics 'only' carry 10% premium

Developing an asic, rather than using an fpga, carries a premium of just 10%, according to sector specialist eSilicon. Hugh Durdan, vp of marketing, believes asics have taken unfair hard knocks from escalating NRE estimates.

"If you look at the $10, 20 or 30million it is now said to cost to develop a solution, only a fraction of that – probably 10% – goes into the cost of the silicon implementation. The rest goes on defining the architecture, implementing the functionality, verifying it and writing all the software.

"To save the 10% it would cost to put all that in an asic by using a more costly solution – higher power, lower performance – probably doesn't make sense. If you must serve a particular application, it's worthwhile to spend that extra 10% and get customised silicon."

Durdan reached his numbers by combining what firms such as his own charge for implementation with the costs of a 90nm mask set and intellectual property, producing a total between $2 and 3m.

• For more on the future of asics, see the Expert Panel on page 19.

Xbox 360 gets upgrade

Microsoft's latest contribution to the gaming console wars is the Xbox 360 Elite. Retailing at just less than $500, it takes advantage of the company's latest manufacturing revisions to add elements such as a 120Gbyte detachable hard drive and an HDMI cable to support 1080p hdtv images.

DAC goes wacky

'Wild and crazy ideas' (WACI) will have special prominence at the 44th Design Automation Conference (www.dac.com), taking place from 4 to 8 June in San Diego.

A special session will consider topics that, whilst on eda's fringe today, could grow in importance. The WACI strand (as in Dick Dastardly's 'Races') features eight papers on topics such as reconfigurable logic using carbon nanotube fets and high performance and lower power electronics on flexible substrates.

Conference general chair Steve Levitan said WACI bridges a gap between traditional DAC sessions (large target attendance, very broad based) and those at events in other disciplines (small attendance, highly focused).

Package combines two techniques for 'truly hermetic' performance

A company from Boston's fast developing nanoelectronics cluster has claimed to be the first to launch 'truly hermetic' packaging technology. Quantum Leap Packaging is claiming a leak rate of less than $5x10^{-8}$ atm cc/s He for its HermeTech quad flats, ahead of a recently established Jedec standard.

The technology is targeted at a wide range of applications, although emerging MEMS, optoelectronics and rf and microwave are the most promising.

QLP's technique combines two proprietary technologies. A high performance organic polymer, Quantech, has features such as low k and low electrical loss at high frequencies. The second is an ultrasonic lid process.